WHAT IS CLAIMED IS:

1. A method of generating a non-integer frequency divided clock signal comprising the steps of:

a) generating a number K of output signal phases P(0) to P(K-1);

b) outputting a present value of an integer index in response to a logic transition of a shift clock signal;

c) selecting one of the K output signal phases P(0) to P(K-1) corresponding to the present value of the integer index as a clock output signal using a glitch free clock selector circuit;

d) clocking a synchronous divide by N counter with the clock output signal generating the non-integer frequency divided clock signal and the shift clock signal;

e) determining when the synchronous divide by N counter has been clocked N times by the clock output signal, wherein the shift clock signal is generated by a transition of the clock output signal following an Nth transition of the clock output signal;

f) receiving an integer fractional divisor having a value less than (K-1); and

g) adding the value of the integer fractional divisor to the present value of the integer index in a modulo (K-1) adding circuit generating a new present value of the integer index.

2. The method of claim 1, wherein the non-integer frequency divided clock signal is used as a feedback clock signal of a phase locked loop circuit having a multiphase voltage controlled oscillator generating the K of equally phased output signals P(0) to P(K-1).

3. The method of claim 1, wherein the K output signal phases P(0) to P(K-1) each have a period T and are progressively phase shifted by an equal amount T/K.

4. A circuit for generating a non-integer frequency divided clock signal that is frequency divided from a clock output signal comprising:

a multiple phase clock having a number K of output signal phases P(0) to P(K-1);

circuitry for outputting a present value M of an integer index in response to a logic transition of a shift clock signal;

glitch free clock selector circuitry for selecting one of the K output signal phases P(M) as a clock output signal in response to the present value M of the integer index;

a synchronous divide by N counter clocked by the clock output signal thereby generating the frequency divided clock signal and the shift clock signal;

circuitry in the divide by N counter for determining when the divide by N counter has been clocked N times by the clock output signal, wherein the shift clock signal is generated by a transition of the clock output signal on a transition following an Nth transition of the clock output signal;

circuitry for receiving an integer fractional divisor having a value S having a value less than (K-1); and

modulo (K-1) adding circuitry for adding the value S to a value of the integer index generating the present value M.

5. The circuit of claim 4, wherein the non-integer value is (N+S/K).

6. The circuit of claim 4, wherein the glitch free clock selector circuitry comprises a K to one Phase multiplexer (MUX) receiving the K clock phase signals and generating a Phase MUX output as P(M), a selected one of the K clock phase signals, in response to a K bit MUX select signal, wherein only one of the K bits is a logic one corresponding to the present value M of the integer index.

7. The circuit of claim 4, wherein the modulo (K-1) adding circuitry comprises:

circuitry for converting S to a K bit phase select signal wherein one of the K bits is a logic one and K corresponds to the value S;

a number of K (K to one) Select MUXs, wherein each input of the K Select MUXs is coupled to one of the K bits of the K bit MUX select signal and the ordering of the coupling for each of the K Select MUXs is rotationally shifted by one from an adjacent Select MUX; and

a K bit register, wherein each register bit stores a state of the output of each of the K Select MUXs in response to the shift clock signal and the outputs of the K bit register form the K bit MUX select signal.

8. The circuit of claim 6, wherein the glitch free clock selector circuitry further comprises a logic circuit for generating the clock output signal as a logic combination of the Phase MUX output and a sequential gating signal that depends on a previous state of the clock output signal.

9. The circuit of claim 4, wherein the K output signal phases P(0) to P(K-1) each have a period T and are progressively phase shifted by an equal amount T/K.

10. A phase locked loop circuit for generating a phase clock signal with a frequency that is a non-integer multiple of a reference clock signal comprising:

a multiphase voltage controlled oscillator (MVCO) generating the phase clock signal as one of a number K of output signal phases P(0) to P(K-1) and the frequency of the phase clock signal is controlled by a control voltage;

a phase frequency detector for comparing a frequency divided clock signal to the reference clock signal and generating a phase/frequency error signal;

circuitry for converting the phase/frequency error signal to the control voltage; and

division circuitry for generating the frequency divided clock signal by frequency dividing a selected one P(M) of the K equally phased output signals by a non-integer value, wherein the division circuitry has circuitry for outputting a present value M of an integer index in response to a logic transition of a shift clock signal, glitch free clock selector circuitry for selecting one of the K equally phased output signals P(M) as a clock output signal in response to the present value M of the integer index, a synchronous divide by N counter clocked by the clock output signal thereby generating the frequency divided clock signal and the shift clock signal, circuitry in the divide by N counter for determining when the divide by N counter has been clocked N times by the clock output signal, wherein the shift clock signal is generated by a transition of the clock output signal on a transition following an Nth transition of the clock output signal, circuitry for receiving an integer fractional divisor having a value S having a value less than (K-1), and modulo (K-1) adding circuitry for adding the value S to a value of the integer index generating the present value M.

11. The phase locked loop circuit of claim 10, wherein the non-integer multiple has a value (N+S/K).

12. The phase locked loop circuit of claim 10, wherein the glitch free clock selector circuitry comprises a K to one Phase multiplexer (MUX) receiving the K clock phase signals and generating a Phase MUX output as P(M), a selected one of the K clock phase signals, in response to a K bit MUX select signal, wherein only one of the K bits is a logic one corresponding to the present value M of the integer index.

13. The phase locked loop circuit of claim 10, wherein the modulo (K-1) adding circuitry comprises:

circuitry for converting S to a K bit phase select signal wherein one of the K bits is a logic one and K corresponds to the value S;

a number of K (K to one) Select MUXs, wherein each input of the K Select MUXs is coupled to one of the K bits of the K bit MUX select signal and the ordering of the coupling for each of the K Select MUXs is rotationally shifted by one from an adjacent Select MUX; and

a K bit register, wherein each register bit stores a state of the output of each of the K Select MUXs in response to the shift clock signal and the outputs of the K bit register form the K bit MUX select signal.

14. The phase locked loop circuit of claim 12, wherein the glitch free clock selector circuitry further comprises a logic circuit for generating the clock output signal as a logic combination of the Phase MUX output and a sequential gating signal that depends on a previous state of the clock output signal.

15. The phase locked loop circuit of claim 10, wherein the K output signal phases P(0) to P(K-1) each have a period T and are progressively phase shifted by an equal amount T/K.

16. A data processing system comprising:

a central processing unit (CPU) clocked by a CPU clock signal;

a random access memory (RAM);

a read only memory (ROM);

an I/O adapter;

a bus system coupling said CPU to said ROM, said communications adapter, said I/O adapter, and said RAM, wherein the CPU clock signal is generated by phase locked loop circuitry as a non-integer multiple of a reference clock signal, the phase locked loop circuitry having a multiphase voltage controlled oscillator (MVCO) generating the CPU clock signal as one of a number K of output signal phases P(0) to P(K-1) and the frequency of the CPU clock signal is controlled by a control voltage;

a phase frequency detector for comparing a frequency divided clock signal to the reference clock signal and generating a phase/frequency error signal;

circuitry for converting the phase/frequency error signal to the control voltage; and

division circuitry for generating the frequency divided clock signal by frequency dividing a selected one P(M) of the K equally phased output signals by a non-integer value, wherein the division circuitry has circuitry for outputting a present value M of an integer index in response to a logic transition of a shift clock signal, glitch free clock selector circuitry for selecting one of the K equally phased output signals P(M) as a clock output signal in response to the present value M of the integer index, a synchronous divide by N counter clocked by the clock output signal thereby generating the frequency divided clock signal and the shift clock signal, circuitry in the divide by N counter for determining when the divide by N counter has been clocked N times by the clock output signal, wherein the shift clock signal is generated by a transition of the clock output signal on a transition following an Nth transition of

the clock output signal, circuitry for receiving an integer fractional divisor having a value S having a value less than (K-1), and modulo (K-1) adding circuitry for adding the value S to a value of the integer index generating the present value M.

17. The data processing system of claim 16, wherein the glitch free clock selector circuitry comprises a K to one Phase multiplexer (MUX) receiving the K clock phase signals and generating a Phase MUX output as P(M), a selected one of the K clock phase signals, in response to a K bit MUX select signal, wherein only one of the K bits is a logic one corresponding to the present value M of the integer index.

18. The data processing system of claim 16, wherein the modulo (K-1) adding circuitry comprises:

circuitry for converting S to a K bit phase select signal wherein one of the K bits is a logic one and K corresponds to the value S;

a number of K (K to one) Select MUXs, wherein each input of the K Select MUXs is coupled to one of the K bits of the K bit MUX select signal and the ordering of the coupling for each of the K Select MUXs is rotationally shifted by one from an adjacent Select MUX; and

a K bit register, wherein each register bit stores a state of the output of each of the K Select MUXs in response to the shift clock signal and the outputs of the K bit register form the K bit MUX select signal.

19. The data processing system of claim 17, wherein the glitch free clock selector circuitry further comprises a logic circuit for generating the clock output signal as a logic combination of the Phase MUX output and a sequential gating signal that depends on a previous state of the clock output signal.

20. The data processing system of claim 16, wherein the K output signal phases P(0) to P(K-1) each have a period T and are progressively phase shifted by an equal amount T/K.